CLAIMS

What is claimed is:

1. ~~A system comprising:~~ See FI

a processor coupled to memory by a bus, the processor having a processor core and a pad ring, the processor core having an independent power supply;

a voltage regulator providing a plurality of voltages and providing the independent power supply;

a clock signal generator providing a clock signal at a plurality of frequencies;

a state machine to coordinate voltage and clock frequency to the processor core; and

an operating system running on the processor, the operating system monitoring an application mix executing in the processor to determine a required frequency, and determining a minimum voltage at which the processor core can operate at the required frequency, wherein the operating system directs the state machine to enter a state in which the required frequency is supplied by the clock signal generator and a closest supported voltage equal to or greater than the minimum voltage is supplied by the voltage regulator.

2. The system of claim 1 wherein the voltage regulator provides one of an idle voltage of a peak voltage.

3. The system of claim 1 wherein the voltage regulator can provide one voltage corresponding to each frequency supported by the clock signal generator.

4. A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

accepting a mesure of processor core performance need of each application currently seeking access to the processor core;

accumulating each measure of processor core performance need to find total current need:

calculating a minimum frequency that will allow the processor core to meet the total current need for the time period:

selecting a lowest supported frequency equal to or greater than the minimum frequency to be a required frequency:

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring;

supplying the required frequency and the minimum supported voltage to the processor core; and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

5. A method of reducing power consumption by a processor core and a pad ring comprising the steps of:

establishing a maximum allowable power consumption;

finding a maximum supported frequency which will allow the processor core to remain below the maximum allowable power consumption at the minimum supported voltage;

selecting a required frequency to be less than or equal to the maximum supported frequency:

finding a minimum supported voltage at which the processor core can operate at the required frequency independent of a voltage required by the pad ring:

supplying the required frequency and the minimum supported voltage to the

processor core: and

dynamically changing the required frequency and the minimum supported voltage supplied responsive to a change in the current application mix.

6. The method of claim 5 wherein a required frequency less than the maximum supported frequency is selected whenever a total processor core performance need of the current application mix can be met by a lower supported frequency

add D5

Add B5

Add A1

Add F1